CLAIMS

What is claimed is:

1. An apparatus for decoding and deinterleaving a received signal, the received signal encoded with two constituent codes and interleaved on a frame by frame basis, the apparatus comprising:

a single constituent code decoder; and

a single common buffer coupled to the single constituent code decoder, the common buffer sized to hold a single frame of received data.

2. The apparatus of claim 1, further comprising:

an address controller coupled to the single common buffer, the address controller generating read and write addresses that cause data to be de-interleaved when read from and written to the common buffer and generating read and write addresses that cause data to be interleaved when read from and written to the common buffer.

3. The apparatus of claim 2, wherein the address controller generates read and write addresses that cause data to be read from the common buffer row by row and to be written to the common buffer column by column to de-interleave the data and generates read and write addresses that cause data to be read from the common buffer column by column and to be written to the common buffer row by row to interleave the data.

4. The apparatus of claim 3, wherein the common buffer is divided into a plurality of sub-buffers and each sub-buffer is a single port memory.

5. The apparatus of claim 4, wherein the address controller is configured to generate a read address for one of the plurality of sub-buffers and a write address for another of the plurality of sub-buffers, the reading and writing of the respective sub-buffers to occur during the same clock cycle.

6. The apparatus of claim 2, wherein the address controller employs a first algorithm to generate read addresses for the common buffer for data input to the constituent code decoder and contemporaneously employs the first algorithm to generate write addresses for the common buffer for data output from the constituent code decoder where the write addresses are offset by a predetermined number of rows from the read addresses when the decoder is decoding the first of the two constituent codes.

7. The apparatus of claim 6, wherein the address controller employs a second algorithm to generate read addresses for the common buffer for data input to the constituent code decoder and contemporaneously employs the second algorithm to generate write addresses for the common buffer for data output from the constituent code decoder where the write addresses are offset by a predetermined number of columns from the read addresses when the decoder is decoding the second of the two constituent codes.

8. The apparatus of claim 7, wherein the employment of the first algorithm to generate write addresses during the decoding of the first of the two constituent codes and employment of the second algorithm to generate read addresses during the decoding of the second of the two constituent codes interleaves the data and the employment of the second algorithm to generate write addresses during the decoding of the second of the two constituent codes and employment of the first algorithm to generate read addresses during the decoding of the first of the two constituent codes de-interleaves the data.

9. The apparatus of claim 8, wherein the address controller is configured to generate read addresses using a one of a row-by-row with column shuffling algorithm and a column-by-column with row shuffling algorithm.

10. The apparatus of claim 9, wherein the received signal is encoded with two constituent codes and interleaved based on a CDMA protocol and wherein the apparatus is employed in a mobile unit deployed within a CDMA-based communication system.

11. A method of decoding and deinterleaving a received signal, the received signal encoded with two constituent codes and interleaved on a frame by frame basis, the method comprising the steps of:

serially decoding the received signal; and

storing received data and decoded data in a single common buffer, the common buffer sized to hold a single frame of received data.

12. The method of claim 11, further comprising the step of:

a) generating read and write addresses that cause data to be de-interleaved when read from and written to the common buffer and generating read and write addresses that cause data to be interleaved when read from and written to the common buffer.

13. The method of claim 12, wherein step a) generates read and write addresses that cause data to be read from the common buffer row by row and to be written to the common buffer column by column to de-interleave the data and generates read and write addresses that cause data to be read from the common buffer column by column and to be written to the common buffer row by row to interleave the data.

14. The method of claim 13, wherein the common buffer is divided into a plurality of sub-buffers and each sub-buffer is a single port memory.

15. The method of claim 14, further comprising the step of generating a read address for one of the plurality of sub-buffers and a write address for another of the plurality of sub-buffers, the reading and writing of the respective sub-buffers occuring during the same clock cycle.

16. The method of claim 12, wherein step a) includes the step of employing a first algorithm to generate read addresses for the common buffer for data input to the constituent code decoder and contemporaneously employing the first algorithm to generate write addresses for the common buffer for data output from the constituent code decoder where the write addresses are offset by a predetermined number of rows from the read addresses when the decoder is decoding the first of the two constituent codes.

17. The method of claim 16, wherein step a) includes the step of employing a second algorithm to generate read addresses for the common buffer for data input to the constituent code decoder and contemporaneously employing the second algorithm to generate write addresses for the common buffer for data output from the constituent code decoder where the write addresses are offset by a predetermined number of columns from the read addresses when the decoder is decoding the second of the two constituent codes.

18. The method of claim 17, wherein the employment of the first algorithm to generate write addresses during the decoding of the first of the two constituent codes and employment of the second algorithm to generate read addresses during the decoding of the second of the two constituent codes interleaves the data and the employment of the second algorithm to generate write addresses during the decoding of the second of the two constituent codes and employment of the first algorithm to generate read addresses during the decoding of the first of the two constituent codes de-interleaves the data.

19. The method of claim 18, wherein step a) includes the step of generating read addresses using a one of a row-by-row with column shuffling algorithm and a column-by-column with row shuffling algorithm.

20. The method of claim 19, wherein the received signal is encoded with two constituent codes and interleaved based on a CDMA protocol and wherein the apparatus is employed in a mobile unit deployed within a CDMA-based communication system.

21. An article of manufacture for use in decoding and deinterleaving a received signal, the received signal encoded with two constituent codes and interleaved on a frame by frame basis, the article of manufacture comprising computer readable storage media including program logic embedded therein that causes control circuitry to perform the steps of:

serially decoding the received signal; and

storing received data and decoded data in a single common buffer, the common buffer sized to hold a single frame of received data.

22. The article of manufacture of claim 21, further performing the step of:

a) generating read and write addresses that cause data to be de-interleaved when read from and written to the common buffer and generating read and write addresses that cause data to be interleaved when read from and written to the common buffer.

23. The article of manufacture of claim 22, wherein step a) generates read and write addresses that cause data to be read from the common buffer row by row and to be written to the common buffer column by column to de-interleave the data and generates read and write addresses that cause data to be read from the common buffer column by column and to be written to the common buffer row by row to interleave the data.

24. The article of manufacture of claim 23, wherein the common buffer is divided into a plurality of sub-buffers and each sub-buffer is a single port memory.

25. The article of manufacture of claim 24, the further performing the step of generating a read address for one of the plurality of sub-buffers and a write address for another of the plurality of sub-buffers, the reading and writing of the respective sub-buffers occuring during the same clock cycle.

26. The article of manufacture of claim 22, wherein step a) includes the step of employing a first algorithm to generate read addresses for the common buffer for data input to the constituent code decoder and contemporaneously employing the first algorithm to generate write addresses for the common buffer for data output from the constituent code decoder where the write addresses are offset by a predetermined number of rows from the read addresses when the decoder is decoding the first of the two constituent codes.

27. The article of manufacture of claim 26, wherein step a) includes the step of employing a second algorithm to generate read addresses for the common buffer for data input to the constituent code decoder and contemporaneously employing the second algorithm to generate write addresses for the common buffer for data output from the constituent code decoder where the write addresses are offset by a predetermined number of columns from the read addresses when the decoder is decoding the second of the two constituent codes.

28. The article of manufacture of claim 27, wherein the employment of the first algorithm to generate write addresses during the decoding of the first of the two constituent codes and employment of the second algorithm to generate read addresses during the decoding of the second of the two constituent codes interleaves the data and the employment of the second algorithm to generate write addresses during the decoding of the second of the two constituent codes and employment of the first algorithm to generate read addresses during the decoding of the first of the two constituent codes de-interleaves the data.

29. The article of manufacture of claim 28, wherein step a) includes the step of generating read addresses using a one of a row-by-row with column shuffling algorithm and a column-by-column with row shuffling algorithm.

30. The article of manufacture of claim 29, wherein the received signal is encoded with two constituent codes and interleaved based on a CDMA protocol and wherein the apparatus is employed in a mobile unit deployed within a CDMA-based communication system.